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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/648,540	08/28/2000	Alexander D. Schapira	246/214	7789

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EXAMINER
GUILL, RUSSELL L

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 03/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/648,540	SCHAPIRA ET AL.	
	Examiner	Art Unit	
	Russell L. Guill	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1,2,8 and 13-17* is/are allowed.

6)☒ Claim(s) *3-7,9-12 and 18* is/are rejected.

7)☒ Claim(s) *12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 August 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is in response to an Amendment filed December 14, 2005. Claims 1 - 18 are pending. Claims 1 - 18 have been examined. Claims 3 - 4, 5 - 7, 9 - 12 and 18 have been rejected. Claims 1 - 2, 8, 13, 14 - 16 and 17 are allowable over the prior art of record.

2. The new Examiner on this application is Russ Guill, as described in the Conclusion section of this Office Action.

Response to Remarks

3. Regarding claim amendments, the Examiner appreciates the amendments to make the claims more readable, and which also clarified the relationships between elements of the claim.

4. Regarding **claims 1, 2 and 8** rejected under 35 USC § 102:

   a. Applicant's arguments, see pages 10 and 11, have been fully considered and are persuasive. Therefore, the rejection of the claims has been withdrawn.

Allowable Subject Matter

5. The previous indication of allowability of **claims 3 - 7, 9 - 12 and 18** is withdrawn in view of the new rejections under 35 USC 112, as described below.

6. **Claim 18** would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

7. **Claims 1 - 2, 8, 13, 14 - 16 and 17** are allowable over the prior art of record.

8. Regarding claim 1, while Nair (U.S. Patent 6,090,149) teaches a circuit design simulator with a stored electronic representation of a circuit design, the circuit design including at least one interface between a digital circuit and an analog circuit the interface comprising a node at which said digital circuit provides an output and at which said analog circuit receives an input, neither Nair taken alone or in combination with the prior art of record discloses the aforementioned circuit design simulator specifically including a circuit design including at least one interface between a digital circuit and an analog circuit, said interface comprising a node at which said digital circuit provides an output and at which said analog circuit receives an input and provides either an output or no output, said digital circuit output taking on any one of several states including a digital high state, digital low state, or high impedance state; and at least one processor for simulating operation of said circuit design, said at least one processor dynamically determining whether to apply said output or said no output to said node according to said digital circuit output state, in combination with the remaining elements and features of the claimed invention. It is for these reasons that the applicant's invention defines over the prior art of record.

9. Regarding claim 8, while Nair (U.S. Patent 6,090,149) teaches a method for simulating electrical operation at an analog/digital interface in a circuit design, neither Nair taken alone or in combination with the prior art of record discloses the aforementioned simulation in a circuit design specifically including identifying an interface between a digital circuit and an analog circuit, said interface comprising a node at which said digital circuit either outputs a digital signal or else presents a high impedance output so as to be effectively isolated from said node, and at which said analog circuit receives an input signal at an input port; adding a conditional output

signal from said input port of said analog circuit to said node, wherein either an output signal or no output signal is applied from said analog circuit to said node; and simulating electrical operation at said interface by applying said output signal from said analog circuit to said node when said digital circuit presents a high impedance output, and applying said no output signal from said analog circuit to said node when said digital circuit presents a digital signal, in combination with the remaining elements and features of the claimed invention. It is for these reasons that the applicant's invention defines over the prior art of record.

10. Regarding claim 13, while Nair (U.S. Patent 6,090,149) teaches a method for simulating a circuit design, neither Nair taken alone or in combination with the prior art of record teaches the aforementioned method for simulating a circuit design specifically including identifying an interface between a plurality of digital circuit outputs and an analog circuit input, wherein each of said plurality of digital circuit outputs can present a high impedance state; modeling said interfaces by adding an output from an analog circuit receiving said analog circuit input to said interface; and simulating electrical operation at said modeled interface by resolving an electrical state of said interface using only the output from the analog circuit when all of said plurality of digital circuit outputs are in a high impedance state, and resolving the electrical state of said interface using one or more of said plurality of digital circuit outputs otherwise, in combination with the remaining elements and features of the claimed invention. It is for these reasons that the applicant's invention defines over the prior art of record.

11. Regarding claim 14, while Nair (U.S. Patent 6,090,149) teaches a mixed analog/digital simulator, neither Nair taken alone or in combination with the prior art of record teaches

the aforementioned mixed analog/digital simulator specifically including a simulation processor; and said simulation processor including a computer-readable medium on which is embodied a set of programmed instructions that cause said simulation processor to simulate the operation of a design circuit, wherein said design circuit includes: a digital circuit having an output; a network electrically coupled to said digital circuit output, said network formed by electrically coupling an input of each of a plurality of circuit blocks at a network input node; said circuit blocks including at least one analog circuit, having an analog circuit input electrically coupled to said network input node; said analog circuit having an input mode of operation for receiving an input signal at said analog circuit input and an output mode of operation for producing an output signal at said analog circuit input; said digital circuit output being applied to said network input node when said digital circuit is in a non-high-impedance state; and said output signal of said analog circuit being applied to said network input node when said digital circuit is in a high-impedance state, in combination with the remaining elements and features of the claimed invention. It is for these reasons that the applicant's invention defines over the prior art of record.

12. Regarding claim 17, while Nair (U.S. Patent 6,090,149) teaches a method of simulating mixed analog/digital systems, neither Nair taken alone or in combination with the prior art of record teaches the aforementioned method of simulating mixed analog/digital systems specifically including transforming an input of an analog circuit into an ioput, said ioput having a conditional output feeding back to a bus, said ioput being operable under a high-impedance input state, and said ioput capable of accepting a digital signal input and producing an analog signal output; electrically coupling said ioput to a digital circuit output and to inputs of a plurality of additional circuits; receiving said digital signal input at said ioput when said digital circuit output is in a non-high-impedance state; and applying said analog signal output at said ioput when said digital circuit

output is in a high-impedance state, in combination with the remaining elements and features of the claimed invention. It is for these reasons that the applicant's invention defines over the prior art of record.

Drawings

13. New corrected drawings in compliance with 37 CFR 1.121(d) are required in this application because the reference numbers are drawn by hand. Applicant is advised to employ the services of a competent patent draftsperson outside the Office, as the U.S. Patent and Trademark Office no longer prepares new drawings. The corrected drawings are required in reply to the Office action to avoid abandonment of the application. The requirement for corrected drawings will not be held in abeyance.

Specification

14. The abstract of the disclosure is objected to because it exceeds 150 words in length. Correction is required. See MPEP § 608.01(b).

Claim Objections

15. **Claim 12** is objected to because of the following informalities: The claim recites, "said plurality of digital circuits." Reference to the previous limitation should remain consistent to avoid any possible confusion or antecedent issues. Appropriate correction is required.

Claim Rejections - 35 USC § 112

16. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of

making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

a. **Claims 3 - 4, 5 - 7, and 9 - 12** are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

i. **Claim 3** appears to describe modeling a digital circuit output as an analog circuit output when the digital circuit output is a high impedance output. This subject matter is described in the claim, however this subject matter does not appear to be described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

ii. **Claim 5** appears to describe modeling a digital circuit output as an analog circuit output when the digital circuit output is a high impedance output. Further, the specification appears to describe resolving contention among multiple digital circuit outputs connected to a bus node such that an analog signal is applied to the bus node only when all digital circuit outputs are in a high impedance state. This subject matter is described in the claim, however this subject matter does not appear to be described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

iii. **Claim 6** appears to describe providing an analog output when only one of a plurality of digital outputs is in a high impedance state. This subject matter does not appear to be described in the specification in such

a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

iv. **Claim 9** appears to describe modeling a digital circuit output as an analog circuit output when the digital circuit output is a high impedance output. Further, the specification appears to describe resolving contention among multiple digital circuit outputs connected to a bus node such that an analog signal is applied to the bus node only when all digital circuit outputs are in a high impedance state. This subject matter does not appear to be described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

v. **Claim 10** appears to describe providing an analog output when only one of a plurality of digital outputs is in a high impedance state. This subject matter does not appear to be described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

vi. **Claim 11** appears to describe providing an analog output when only one of a plurality of digital outputs is in a high impedance state. This subject matter does not appear to be described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

vii. **Claims 4, 7 and 12** are rejected based on their dependency on their respective intermediate and parent claims which are rejected under 35 U.S.C. 112, first paragraph.

17. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

a. **Claims 3 - 4, 5 - 7, 9 - 12 and 18** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

i. Regarding **claim 3**, in the second limitation, the claim describes modeling said output (from a digital circuit) as an analog output signal from an analog circuit when the output is in a high impedance state. The output cannot both be in a high impedance state and in an analog signal state. It is not possible to determine the metes and bounds of the claim. Correction or amendment is required.

ii. Regarding **claim 5**, in the second limitation, the claim describes modeling at least one of said outputs (from digital circuits) as an analog output signal from an analog circuit when said at least one output is in a high impedance state. The output cannot both be in a high impedance state and in an analog signal state. It is not possible to determine the metes and bounds of the claim. Correction or amendment is required.

iii. Regarding **claim 9**, in the second limitation, the claim describes modeling at least one of said outputs (from digital circuits) as an analog output signal from an analog circuit when said at least one output is in a high impedance state. The output cannot both be in a high impedance state and in an analog signal state. It is not possible to determine the metes and bounds of the claim. Correction or amendment is required.

iv. Regarding **claim 18**, the Examiner cannot determine whether the new limitation is intended to entirely replace the electrically coupling limitation in claim 17, or whether the new limitation is intended to be in addition to the electrically coupling limitation in claim 17. Further, the

Examiner cannot determine whether the recited "to inputs of a plurality of additional circuits" of claim 17 is intended to still be part of the limitation. The metes and bounds of the claim cannot be determined. Correction or amendment is required.

v. **Claims 4, 6 - 7 and 10 - 12** are rejected based on their dependency on their respective intermediate and parent claims which are rejected under 35 U.S.C. 112, second paragraph.

Conclusion

18. The prior art made of record and not relied upon is considered pertinent to the applicant's disclosure:

a. Goody, Roy W.; "MicroSim PSpice for Windows", second edition, 1998, Prentice Hall; teaches an output of a logic device connected to the input of an analog op amp device with output feedback from the analog device back to the digital output node/analog input node.

19. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Russell L. Guill whose telephone number is 571-272-7955. The examiner can normally be reached on Monday - Friday 9:30 AM - 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul Rodriguez can be reached on 571-272-3753. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Any inquiry of a general nature or relating to the status of this application should be directed to the TC2100 Group Receptionist: 571-272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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RG

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